IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)
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MURAKAMI et al.	)
	)
Application Number: To be Assigned	)
	)
Filed: Concurrently herewith	)
	)
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF	)
	)
Attorney Docket No. TSUT.0028	)

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

The above-referenced application is a Continuation of U.S. Application No. 10/288,448 filed on November 6, 2002. It includes the same disclosure as U.S. patent application Serial No. 10/288,448.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application, pursuant to 37 CFR § 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

This Information Disclosure Statement is submitted with the above-captioned U.S. Continuation Application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,

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February 11, 2004

Form PTO 1449 U.S. Department of commerce Patent and Trademark Office Information Disclosure Statement by Applicant	ATTY. DOCKET NUMBER **TSUT.0028**	SERIAL NUMBER **To be assigned**
	APPLICANT **MIRAKAMI et al.**	
	FILING DATE **Concurrently herewith**	GROUP

U.S. Patent Documents

Examiner Initial		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	**	5,591,681	1/7/97	Wristers et al			6/3/94
	**	6,235,590	5/22/01	Daniel et al			12/18/98
	**	6,258,673	7/10/01	Houlihan et al			12/22/99
	**	6,168,980	1/2/01	Yamazaki.et al			9/26/96
	**	6,037,639	3/14/00	Ahmad			6/9/97
	**	5,554,871	9/10/96	Yamashita et al			6/7/95
	**	6,232,244	5/15/01	Ibok			5/1/00
	**	6,051,510	4/18/00	Fulford, Jr. et al			5/2/97
	**	5,702,988	12/30/97	Liang			5/2/96
	**	5,629,221	5/13/97	Chao et al			11/24/95
	**	5,464,783	11/7/95	Kim et al			2/2/95
	**	4,554,726	11/26/85	Hellenius et al			4/17/84

Foreign Patent Documents

Examiner Initial		DOCUMENT NUMBER	FILING DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	No

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

	*	N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai and T. Horiuchi, "the Impact of Bias Temperature Instability for Direct-Tunneling Ultra-thin GTE Oxide on MOSFET Scaling", 1999 Symposium on VLSI Technology Digest of Technical papers, pp. 73-74

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant

PTO 1449

* **Filed by Applicant in Parent**

** **Cited by Examiner in Parent**